

REMARKS

This is intended as a full and complete response to the Office Action dated November 15, 2005, having a shortened statutory period for response set to expire on February 15, 2006. Please reconsider the claims pending in the application for reasons discussed below. Claims 8-13, 15-23 and 25-27 remain pending in the application and are shown above. Claims 8-13, 15-23 and 25-27 stand rejected by the Examiner. Claims 31-32 have been added. Reconsideration of the claims is requested for reasons presented below.

DOUBLE PATENTING

Claims 8-11 and 16-19 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 7-8, 10, 12, and 19-20 of co-pending Application No. 10/666,317 in view of *Tao et al.* (U.S. Patent No. 6,620,631), in further view of *Tao et al.* (U.S. Patent No. 6242,350).

The Applicants will file a provisional terminal disclaimer to resolve the present double patenting rejection if and when one of the rejected claims is allowed.

CLAIM REJECTIONS**35 U.S.C. §103(a)**

Claim 8-13, 15-23, and 25-27 stand rejected under 35 USC § 103(a) as being unpatentable over United States Patent No. 6,242,350 issued June 5, 2001, to *Tao, et al.* (hereinafter referred to as "Tao I") in further view of United States Patent No. 6,242,350 issued June 5, 2001 to *Tao et al.*, (hereinafter referred to as "Tao II").

In response, Applicants have amended independent claims 8 and 16 to more clearly recite aspects of the invention. The rejection is respectfully traversed. Independent claims 8 and 16, as amended, recite limitations not taught, shown or suggested by *Tao I* and *Tao II* alone or in combination.

Tao I teaches a method to compensate for a deviation of the patterned masking layers 14a, 14b, 14c, 14d, and 14e measured linewidth from a patterned masking layer target linewidth. The patterned masking layers linewidth are measured, and then the

measurements of the patterned masking layers are compared with a target linewidth in order to determine a deviation. Then based on the deviation, a plasma etch parameter is adjusted to provide for a closer linewidth to the target (generally column 8, line 62 to column 9, line 15). *Tao I*'s teaching is limited to measuring a processed mask layer and comparing the processed mask layer to a target mask layer and adjusting an etch variable for a closer process. The Examiner concedes that *Tao I* does not teach, show, or suggest at least one of compacting or removing at least a portion of a post-etch residue formed on sidewalls of the etched structures. Also, *Tao I* does not teach, show, or suggest etching a material layer on a substrate after trimming the patterned mask on the substrate, measuring a thickness of post-etch residue and compacting or removing at least a portion of the post-etch residue formed on sidewalls of the etched structures based on the thickness of the post-etch residue, measuring dimensions of etched structures formed on a substrate during etch step of the material layer, and then adjusting the trimming process of the patterned mask or adjusting the etch process of the material layer based on the measurements of dimensions of the etched structures as recited by claim 8.

Tao II does not cure the deficiencies of *Tao I*. *Tao II* teaches a method for removing photoresist and polymer residues from the surface of an integrated circuit wafer after plasma etch process of a gate electrode structure with minimal plasma damage and minimal loss of gate oxide (column 2, lines 57-61). *Tao II* does not teach a method or an apparatus for measuring a patterned mask or an etch structure in order to adjust and provide for a controlled accuracy or repeatability. Importantly, *Tao II* does not teach, show, or suggest measuring a thickness of post-etch residue and compacting or removing at least a portion of the post-etch residue formed on sidewalls of the etched structures based on the thickness of the post-etch residue. Thus, *Tao II* does not teach, show, or suggest measuring dimensions of elements of a patterned mask on one substrate, trimming the patterned mask on the substrate using a process recipe based on the measurements of the dimensions of the patterned mask, etching a material layer on a substrate after trimming the patterned mask on the substrate, measuring a thickness of post-etch residue and compacting or removing at least a portion of the post-etch residue formed on sidewalls of the etched structures based on

APPM/008327/ETCH/SILICON/JB
Serial No. 10/690,318
Page 8 of 9

the thickness of the post-etch residue, measuring dimensions of etched structures formed on a substrate during etch step of the material layer, and then adjusting the trimming process of the patterned mask or adjusting the etch process of the material layer based on the measurements of dimensions of the etched structures as recited by claim 8.

Thus, the combination of *Tao I* and *Tao II* does not teach or suggest (a) a method for controlling accuracy and repeatability of an etch process, comprising providing a batch of substrates, each substrate having a patterned mask formed on a film stack comprising at least one material layer, (b) measuring dimensions of elements of the patterned mask on at least one substrate of the batch of substrates, (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b) then, (d) etching the at least one material layer on the at least one substrate, (e) measuring a thickness of post-etch residue and at least one of compacting or removing at least a portion of the post-etch residue formed on sidewalls of the etched structures based on the thickness of the post-etch residue, (f) measuring dimensions of etched structures formed on the at least one substrate during step (d); and (g) adjusting the process recipe of step (c) or/and the process recipe of step (d), based on the measurements performed at step (f) as recited by claim 8, from which claims 9-13, and 15 depend. Therefore, Applicant submits that independent claim 8 and dependent claims 9-13, and 15 are patentable over *Tao I* in view of *Tao II*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

In addition, claim 16 contains substantially the same language of as claim 8. Therefore as discussed above, the combination of *Tao I* and *Tao II* does not teach, show, or suggest a method for controlling accuracy and repeatability during formation of a gate structure of a field effect transistor, comprising (a) providing a batch of substrates, each substrate having a patterned mask formed on a gate electrode layer of the gate structure, (b) measuring dimensions of elements of the patterned mask on at least one substrate of the batch of substrates, (c) trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed at step (b) then, (d) etching the gate electrode layer on the at least one substrate, (e)

APPM/008327/ETCH/SILICON/JB
Serial No. 10/690,318
Page 9 of 9

measuring a thickness of post-etch residue and at least one of compacting or removing at least the portion of post-etch residue formed on sidewalls of the etched structures based on the thickness of the post-etch residue, (f) measuring dimensions of etched gate electrode structures formed on the at least one substrate during step (d), and (g) adjusting the process recipe of step (c) or/and the process recipe of step (d) based on the measurements performed at step (f) as recited in claim 16. Therefore, Applicants submit that independent claim 16 and dependent claims 17-23, and 25-27 are patentable over *Tao I* in view of *Tao II*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

NEW CLAIMS

New claim 31-32 have been added. The Applicants believe that claims 31-32 are fully supported by the specification and no new matter has been entered. Claims 31-32 are patentable over the art of record at least by their respective dependencies from claims 8 and 16. Thus, the Applicants respectfully request allowance of claims 31-32.

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



Keith M. Tackett,
Registration No. 32,008
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant(s)